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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/853,335 | STRONGIN ET AL. | |
| | Examiner | Art Unit | |
| | XUAN M. THAI | 2111 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *24 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-13 and 15-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 15-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This is in response Amendment filed on May 24, 2004. Claim 14 has been canceled. Claims 1-13 and 15-57 are currently pending in this application.

### *Claim Rejections - 35 USC § 112*

2. The amendments to claims 3, 9 and 21 have obviated the 35 USC 112 rejection.

### *Double Patenting*

3. The cancellation of claim 14 obviated the double patenting rejection.

### *Claim Rejections - 35 USC § 102*

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-2, 4-8, 10-15 and 30-57 are rejected under 35 U.S.C. 102(e) as being anticipated by Moriarty et al. (USPN 6,446,149; Moriarty).

As per claim 1, Moriarty discloses a bus interface logic (bridge) configured with a storage location (address space / semaphore memory cell; abstract) configured to store a master mode bit (semaphore memory cell; abstract; col. 2, lines 16-23), wherein the bus interface logic is configured to exchange data only with a master device that caused the master mode bit to be set when the master mode bit is set (col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67; col. 11, lines 35-46).

As per claim 2, Moriarty discloses the bus interface logic of claim 1 further configured to flush output buffers in response to the master mode bit being reset (col. 9, lines 44-51).

As per claim 4, Moriarty discloses the bus interface logic of claim 1, wherein the storage location is further configured to store one or more addresses (col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67), and wherein the bus interface logic is configured to exchange data only with the one or more addresses (col. 11, lines 35-46).

As per claim 5, Moriarty discloses the bus interface logic of claim 4, wherein the one or more addresses comprise an address range (e.g. col. 11, lines 20-25), wherein the bus interface logic is configured to exchange data only within the address range.

As per claim 6, Moriarty discloses the bus interface logic of claim 1, wherein the storage location is further configured to store one or more addresses (col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67), and wherein the bus interface logic is configured not to exchange data with the one or more addresses (e.g. col. 9, lines 44-47).

As per claim 7, Moriarty discloses a computer system, comprising: a master device (busmaster) configured to set and reset a master mode bit (read/write; col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67); and one or more bus interface logics (bridges), each configured with a storage location configured to store the master mode bit (address space/ semaphore memory cell; abstract; col. 2, lines 16-23), wherein the bus interface logics are configured to exchange data only with the master device when the master mode bit is set (col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67; col. 11, lines 35-46).

As per claim 8, Moriarty computer system of claim 7, wherein the bus interface logics are further configured to flush output buffers in response to the master mode bit being reset (col. 9, lines 56-61; col. 11, lines 37-44).

As per claim 10, Moriarty discloses the computer system of claim 7, wherein the storage location is further configured to store one or more addresses, and wherein the one or more bus interface logics are configured to exchange data only with the one or more addresses (col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67).

As per claim 11, Moriarty discloses the computer system of claim 10, wherein the one or more addresses comprise an address range (col. 11, lines 20-25), wherein the one or more bus interface logics are configured to exchange data only within the address range.

As per claims 12 and 14, Moriarty discloses the computer system of claim 10, wherein the master device is further configured to store the one or more addresses in the storage location along with the master mode bit (e.g. col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67).

As per claim 13, Moriarty discloses the computer system of claim 7, wherein the storage location is further configured to store one or more addresses (col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67), and wherein the one or more bus interface logic are configured not to exchange data with the one or more addresses (e.g. col. 9, lines 44-47).

As per claim 15, Moriarty inherently discloses a processor configured to exchange data through the one or more bus interface logics when the master mode bit is not set; and wherein the one or more bus interface logics are further configured not to exchange data for the processor when the master mode bit is set. In that the bridges of the Moriarty system functions for normal data exchange between plurality of bus masters and targets when the master mode bit is not set. However, when the master mode bit is set, only the bus master with exclusive access as indicated by the master mode bit being set would be able to exchange data through the bridge(s).

As per claims 30 and 47, Moriarty discloses a method and computer instructions (algorithm; col.8, lines 1 et seq.) of operating a computer system, the method comprising: setting a master mode bit for a bus interface logic (read; col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67); passing a data request through the bus interface logic only for a specified device (col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67; col. 11, lines 35-46); receiving data in response to the data request from the specified device (col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67; col. 11, lines 35-46) and resetting the master mode bit (write; col. 8, lines 18-67).

As per claims 31 and 48, Moriarty further discloses setting a master mode bit in another bus interface logic (col. 12, lines 52-56); and passing the data request from the another bus interface logic to the bus interface logic only for the specified device (col. 10, lines 21-67).

As per claims 32 and 49, Moriarty further discloses the method wherein setting a master mode bit for a bus interface logic comprises a master device setting the master mode bit for the bus interface logic (e.g. col. 7, lines 28-34); and wherein passing the data request through the bus interface logic only for the specified device further comprises the master device providing the data request through the bus interface logic only for the specified device (col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67; col. 10, lines 21-67; col. 11, lines 35-46).

As per claims 33 and 50, Moriarty further discloses the method comprising: making an attempt to access the bus interface logic; and rejecting the attempt to access the bus interface logic by other than the master device or the specified device, when the master mode bit is set (read/busy; e.g. col. 7, lines 28-34) .

As per claims 34 and 51, Moriarty further discloses the method comprising: resetting (write) the master mode bit; and flushing buffers of the bus interface logic in response to resetting the master mode bit (col. 9, lines 44-51; col. 11, lines 35-46).

As per claims 35 and 52, Moriarty discloses the method of claim 34, further comprising: making an attempt to access the bus interface logic; and accessing the bus interface logic in response to making the attempt to access the bus interface logic by other than the master device or the specified device, after the master mode bit is reset (read by another master; e.g. col. 7, lines 28-34; col. 9, lines 56-61).

As per claims 36 and 53, Moriarty further discloses the method comprising: storing one or more address locations along with the master mode bit for the bus interface logic (col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67).

As per claims 37 and 54, Moriarty further discloses the method comprising: restricting data transmissions only to the one or more address locations (e.g. col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67).

As per claims 38 and 55, Moriarty further discloses the method comprising: restricting data transmissions only to within an address range defined by the one or more address locations (e.g. col. 11, lines 20-25).

As per claims 39 and 56, Moriarty further discloses the method comprising: restricting data transmissions from the one or more address locations (e.g. col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67).

As per claims 40 and 57, Moriarty further discloses the method comprising: restricting data transmissions from within an address range defined by the one or more address locations (e.g. col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67).

As per claim 41, Moriarty discloses a computer system, comprising: means (address space/semaphore memory cells) for storing an indicator of a master mode; means (bridge) for restricting data transfers when the indicator of the master mode is set; means (address space/semaphore memory cells; busmaster(s)) for resetting the indicator of the master mode (write; e.g. col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67).

As per claim 42, Moriarty discloses a computer system, comprising: means (busmaster; read) for setting a master mode bit for a bus interface logic; means (bridge) for passing a data request through the bus interface logic only for a specified device; means (bridge; gateway) for receiving data in response to the data request from the specified device; and means (busmaster; write) for resetting the master mode bit (e.g. col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67).

As per claim 43, Moriarty discloses the computer system of claim 42, further comprising: means for setting a master mode bit in another bus interface logic (col. 12, lines 52-56); and means for passing the data request from the another bus interface logic to the bus interface logic only for the specified device (col. 10, lines 21-67).

As per claim 44, Moriarty discloses the computer system of claim 42, further comprising: means (bridge) for rejecting (busy) an attempt to access the bus interface logic by other than the master device or the specified device, when the master mode bit is set (e.g. col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67).

As per claim 45, Moriarty discloses the computer system of claim 42, further comprising: means for resetting the master mode bit (busmaster; write); and means for flushing buffers of the bus interface logic in response to resetting the master mode bit (col. 9, lines 44-51; col. 11, lines 35-46).

As per claim 46, Moriarty discloses the computer system of claim 45, further comprising: means for accessing the bus interface logic in response to making an attempt to access the bus interface logic by other than the master device or the specified device, after the master mode bit is reset (read by another master; e.g. col. 7, lines 28-34; col. 9, lines 56-61).

6. Claims 1-2, 4-8, 10-15, 30-31 and 47-48 are rejected under 35 U.S.C. 102(e) as being anticipated by Parks (USPN 6,356,983).

As per claims 1, 30 and 47, Parks discloses system and method comprising: a bus interface logic (repeater and repeater control & status registers; fig. 3, 4 or 10) configured with a storage location (status registers or ID registers) configured to store a master mode bit (initiator ID; col. 8, lines 26-28 and 40-67), wherein the bus interface logic is configured to exchange data only with a master device that caused the master mode bit to be set when the master mode bit is set (col. 8, lines 26-28 and 40-67).

As per claim 2, Parks discloses the bus interface logic of claim 1, further configured to flush output buffers in response to the master mode bit being reset (col. 9, lines 44-51).

As per claim 4, 31 and 48, Parks discloses wherein the storage location is further configured to store one or more addresses (col. 8, lines 26-28 and 40-67), and wherein the bus interface logic is configured to exchange data only with the one or more addresses (col. 8, lines 26-28 and 40-67).

As per claim 5, Parks discloses the bus interface logic of claim 4, wherein the one or more addresses comprise an address range (ID0-ID7 or ID0-ID15), wherein the bus interface logic is configured to exchange data only within the address range.

As per claim 6, Parks discloses the bus interface logic of claim 1, wherein the storage location is further configured to store one or more addresses (ID0-ID7 or ID0-

ID15), and wherein the bus interface logic is configured not to exchange data with the one or more addresses (e.g. col. 14, lines 14-51).

As per claim 7, Parks discloses a computer system, comprising: a master device (e.g. initiator) configured to set and reset a master mode bit (initiator ID; col. 8, lines 26-28 and 40-67); and one or more bus interface logics, each configured with a storage location configured to store the master mode bit (repeater and repeater control & status registers; fig. 3, 4 or 10; initiator ID; col. 8, lines 26-28 and 40-67), wherein the bus interface logics are configured to exchange data only with the master device when the master mode bit is set (col. 8, lines 26-28 and 40-67).

As per claim 8, Parks computer system of claim 7, wherein the bus interface logics are further

configured to flush output buffers in response to the master mode bit being reset (col. 9, lines 44-51).

As per claim 10, Parks discloses the computer system of claim 7, wherein the storage location is further configured to store one or more addresses, and wherein the one or more bus interface logics are configured to exchange data only with the one or more addresses (col. 8, lines 26-28 and 40-67).

As per claim 11, Parks discloses the computer system of claim 10, wherein the one or more addresses comprise an address range (ID0-ID7 or ID0-ID15), wherein the one or more bus interface logics are configured to exchange data only within the address range (col. 8, lines 26-28 and 40-67).

As per claims 12 and 14, Parks discloses the computer system of claim 10, wherein the master device is further configured to store the one or more addresses in the storage location along with the master mode bit (e.g. col. 8, lines 26-28 and 40-67).

As per claim 13, Parks discloses the computer system of claim 7, wherein the storage location is further configured to store one or more addresses, and wherein the one or more bus interface logic are configured not to exchange data with the one or more addresses (e.g. col. 14, lines 14-51).

As per claim 15, Parks discloses the computer system of claim 7, further comprising: a processor configured to exchange data through the one or more bus interface logics when the master mode bit is not set; and wherein the one or more bus interface logics are further configured not to exchange data for the processor when the master mode bit is set (col. 8, lines 26-28 and 40-67 and col. 14, lines 14-51).

7. Claims 1-15 and 30-57 are rejected under 35 U.S.C. 102(e) as being anticipated by Scholhamer et al. (USPN 6636921; Scholhamer).

As per claims 1 and 3, Scholhamer discloses a bus interface logic (col. 7, lines 3-10) configured with a storage location (303) configured to store a master mode bit, wherein the bus interface logic is configured to exchange data only with a master device that caused the master mode bit to be set when the master mode bit is set (col. 9, lines 19-33; col. 12, lines 50-53; see also Table 5).

As per claim 2, Scholhamer discloses the bus interface logic of claim 1, further configured to flush output buffers in response to the master mode bit being reset

As per claim 4, Scholhamer discloses the bus interface logic of claim 1, wherein the storage location is further configured to store one or more addresses (col. 9, lines 19-33), and wherein the bus interface logic is configured to exchange data only with the one or more addresses.

As per claim 5, Scholhamer discloses the bus interface logic of claim 4, wherein the one or more addresses comprise an address range (Node Presence vector), wherein the bus interface logic is configured to exchange data only within the address range (col. 9, lines 19-33).

As per claim 6, Scholhamer discloses the bus interface logic of claim 1, wherein the storage location is further configured to store one or more addresses, and wherein the bus interface logic is configured not to exchange data with the one or more addresses (e.g. col. 16, lines 4-6).

As per claims 7 and 9, Scholhamer discloses a computer system, comprising: a master device (e.g. Nodes and Node Processors) configured to set and reset a master mode bit (col. 7, lines 3-10); and one or more bus interface logics, each configured with a storage location configured to store the master mode bit (col. 6, lines 35-67; col. 7, lines 3-10), wherein the bus interface logics are configured to exchange data only with the master device when the master mode bit is set (col. 9, lines 19-33; col. 12, lines 50-53; see also Table 5).

As per claim 8, Scholhamer discloses the computer system of claim 7, wherein the bus interface logics are further configured to flush output buffers in response to the master mode bit being reset.

As per claim 10, Scholhamer discloses the computer system of claim 7, wherein the storage location is further configured to store one or more addresses, and wherein the one or more bus interface logics are configured to exchange data only with the one or more addresses (col. 9, lines 19-33).

As per claim 11, Scholhamer discloses the computer system of claim 10, wherein the one or more addresses comprise an address range (Node Presence vector), wherein the one or more bus interface logics are configured to exchange data only within the address range (col. 9, lines 19-33).

As per claims 12 and 14, Scholhamer discloses the computer system of claim 10, wherein the master device is further configured to store the one or more addresses in the storage location along with the master mode bit (col. 6, lines 35-67; col. 7, lines 3-10).

As per claim 13, Scholhamer discloses the computer system of claim 7, wherein the storage location is further configured to store one or more addresses, and wherein the one or more bus interface logic are configured not to exchange data with the one or more addresses (e.g. col. 16, lines 4-6).

As per claim 15, Scholhamer discloses the computer system of claim 7, further comprising: a processor configured to exchange data through the one or more bus interface logics when the master mode bit is not set; and wherein the one or more bus interface logics are further configured not to exchange data for the processor when the master mode bit is set (col. 9, lines 54-55).

As per claims 30 and 47, Scholhamer discloses a method and computer instructions (operations) of operating a computer system, the method comprising: setting a master mode bit for a bus interface logic (col. 6, lines 35-67; col. 7, lines 3-10); passing

a data request through the bus interface logic only for a specified device (col. 9, lines 19-33; col. 12, lines 50-53; see also Table 5); receiving data in response to the data request from the specified device (col. 9, lines 19-33; col. 12, lines 50-53; see also Table 5) and resetting the master mode bit (col. 7, lines 3-10).

As per claims 31 and 48, Scholhamer further discloses setting a master mode bit in another bus interface logic; and passing the data request from the another bus interface logic to the bus interface logic only for the specified device (col. 9, lines 19-33; col. 12, lines 50-53; see also Table 5).

As per claims 32 and 49, Scholhamer further discloses the method wherein setting a master mode bit for a bus interface logic comprises a master device setting the master mode bit for the bus interface logic (col. 9, lines 19-33; col. 12, lines 50-53; see also Table 5); and wherein passing the data request through the bus interface logic only for the specified device further comprises the master device providing the data request through the bus interface logic only for the specified device (col. 9, lines 19-33; col. 12, lines 50-53; see also Table 5).

As per claims 33 and 50, Scholhamer further discloses the method comprising: making an attempt to access the bus interface logic; and rejecting the attempt to access the bus interface logic by other than the master device or the specified device, when the master mode bit is set (request and retry; col. 9, lines 19-33; col. 12, lines 50-53; see also Table 5) .

As per claims 34 and 51, Scholhamer further discloses the method comprising: resetting the master mode bit; and flushing buffers of the bus interface logic in response to resetting the master mode bit.

As per claims 35 and 52, Scholhamer discloses the method of claim 34, further comprising: making an attempt to access the bus interface logic; and accessing the bus interface logic in response to making the attempt to access the bus interface logic by other than the master device or the specified device, after the master mode bit is reset (uncached; col. 12, lines 14-15).

As per claims 36 and 53, Scholhamer further discloses the method comprising: storing one or more address locations along with the master mode bit for the bus interface logic (col. 6, lines 35-67; col. 7, lines 3-10).

As per claims 37 and 54, Scholhamer further discloses the method comprising: restricting data transmissions only to the one or more address locations (e.g. col. 6, lines 35-67; col. 7, lines 3-10; col. 9, lines 19-33 col. 9, lines 54-55; col. 16, lines 4-6).

As per claims 38 and 55, Scholhamer further discloses the method comprising: restricting data transmissions only to within an address range defined by the one or more address locations (e.g. col. 6, lines 35-67; col. 7, lines 3-10; col. 9, lines 19-33 col. 9, lines 54-55; col. 16, lines 4-6).

As per claims 39 and 56, Scholhamer further discloses the method comprising: restricting data transmissions from the one or more address locations (e.g. col. 6, lines 35-67; col. 7, lines 3-10; col. 9, lines 19-33 col. 9, lines 54-55; col. 16, lines 4-6).

As per claims 40 and 57, Scholhamer further discloses the method comprising: restricting data transmissions from within an address range defined by the one or more address locations (e.g. col. 6, lines 35-67; col. 7, lines 3-10; col. 9, lines 19-33 col. 9, lines 54-55; col. 16, lines 4-6).

As per claim 41, Scholhamer discloses a computer system, comprising: means (303) for storing an indicator of a master mode; means (e.g. 300) for restricting data transfers when the indicator of the master mode is set; means (e.g. 301) for resetting the indicator of the master mode (col. 9, lines 19-33; col. 12, lines 50-53; see also Table 5).

As per claim 42, Scholhamer discloses a computer system, comprising:

means (301) for setting a master mode bit for a bus interface logic;

means (301) for passing a data request through the bus interface logic only for a specified device;

means (301) for receiving data in response to the data request from the specified device; and

means (301) for resetting the master mode bit (col. 9, lines 19-33; col. 12, lines 50-53; see also Table 5).

As per claim 43, Scholhamer discloses the computer system of claim 42, further comprising: means for setting a master mode bit in another bus interface logic; and means for passing the data request from the another bus interface logic to the bus interface logic only for the specified device.

As per claim 44, Scholhamer discloses the computer system of claim 42, further comprising: means (301) for rejecting (retry) an attempt to access the bus interface logic by other than the master device or the specified device, when the master mode bit is set (col. 9, lines 19-33; col. 12, lines 50-53; see also Table 5).

As per claim 45, Scholhamer discloses the computer system of claim 42, further comprising: means for resetting the master mode bit; and means for flushing buffers of the bus interface logic in response to resetting the master mode bit.

As per claim 46, Scholhamer discloses the computer system of claim 45, further comprising: means (Node bridge) for accessing the bus interface logic in response to making an attempt to access the bus interface logic by other than the master device or the specified device, after the master mode bit is reset (uncached; col. 12, lines 14-15).

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moriarty et al. (USPN 6,446,149; Moriarty) in view of Kao et al. (USPN 6,651,168; Kao).

As per claims 16 and 17, Moriarty discloses the claimed invention except for the master device comprises a crypto processor and security hardware. Kao teaches authentication framework for multiple authentication processes and mechanisms to enable a computer system to authenticate a user with a selected one of the plurality of authentication processes (Abstract). It would have been obvious to one of the ordinary skill in the art to incorporate the teachings of Kao in the Moriarty system as taught by Kao in order to achieve the claimed invention. In doing so would provide flexibility in providing diverse user authentication mechanisms and processes for a stand-alone computer system of for a distributed computer network (col. 2, lines 45-54).

11. Claims 18, 19 and 21-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moriarty et al. (USPN 6,446,149; Moriarty) in view of Kao et al. (USPN 6,651,168; Kao).

As per claims 18, 21, 28 and 29, Moriarty discloses the claimed invention including a master device (busmaster); at least a first bus interface logic (bridge) coupled to the master device, wherein the first bus interface logic comprises a first storage location (address space/ semaphore memory cell) for storing a first master mode bit; and at least a second bus interface logic (bridge) coupled to the device, wherein the first bus interface logic (bridge) comprises a second storage location (semaphore memory cells) for storing a second master device mode bit; wherein the master device is configured to cause to be set the first master mode bit in the first storage location and the second master mode bit in the second storage location; wherein the first bus interface logic is configured to exchange data only between the master device and the second bus interface logic when

the first master mode bit is set; and wherein the second bus interface logic is configured to exchange data only between the device and the first bus interface logic when the second master mode bit is set (col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67; col. 10, lines 21-67; col. 11, lines 35-46; col. 12, lines 52-56). Moriarty does not disclose a device, different from the master device, configured to provide authentication data to the master device and a cryptoprocessor and security hardware.

Kao teaches authentication framework for multiple authentication processes and mechanisms to enable a computer system to authenticate a user with a selected one of the plurality of authentication processes (Abstract). It would have been obvious to one of the ordinary skill in the art to incorporate the teachings of Kao in the Moriarty system as taught by Kao in order to achieve the claimed invention. In doing so would provide flexibility in providing diverse user authentication mechanisms and processes for a stand-alone computer system of for a distributed computer network (col. 2, lines 45-54).

As per claim 19, wherein the master device is configured to set and reset the first and second master mode bits (Moriarty; read/write; col. 8, lines 18-67).

As per claim 20, wherein the first and second bus interface logics are further configured to flush output buffers in response to the first and second master mode bits being reset (Moriarty; write; col. 9, lines 44-51 and col. 11, lines 35-46).

As per claim 22, wherein the first and second storage locations are configured t store one or more addresses, and the first and second bus interface logics are configured to exchange data only with one or more addresses as stored therein (Moriarty; col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67).

As per claim 23, wherein the one or more addresses comprise an address range, wherein the first and second bus interface logics are configured to exchange data only within the address range (Moriarty; e.g. col. 11, lines 20-25).

As per claim 24, wherein the master device is further configured to store the one or more addresses in the first and second storage locations along with the first and second master mode bits (Moriarty; e.g. col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67).

As per claim 25, wherein the first and second storage locations are further configured to store one or more addresses, and wherein the first and second bus interface logics are each configured not to exchange data with the one or more addresses stored therein (Moriarty; e.g. col. 9, lines 44-47).

As per claim 26, wherein the master device is further configured to store the one or more addresses in the first and second storage locations along with the first and second master mode bits (Moriarty; e.g. col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67).

As per claim 27, a processor configured to exchange data through the first and second bus interface logics when the first and second master mode bits are not set; and wherein the first and second bus interface logics are each further configured not to exchange data for the processor when the first and second master mode bits, respectively, are set. The limitation would be within the inherent teachings of Moriarty in that in the Moriarty system when the master mode bits are not set, normal data transfer over the bus through the bridges can take place. However, when the master mode bits are set, only the bus master(s) with exclusive access can exchange data through the bridge.

***Response to Arguments***

12. Applicant's arguments filed on May 24, 2004 have been fully considered but they are not persuasive. Applicant argued that the cited references failed to teach or suggest a master mode bit, a bit that indicates that one or more bus interface logics or other devices will be used to establish a secure transmission channel between a master mode logic and a data input device while operating outside the operating system.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a master mode bit, a bit that indicates that one or more bus interface logics or other devices will be used to establish a secure transmission channel between a master mode logic and a data input device while operating outside the operating system) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). In so far as the prior art being cited, they disclose or teach explicitly or inherently all the limitations as claimed as detailed supra.

***Conclusion***

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to XUAN M. THAI whose telephone number is 703-308-2064. The examiner can normally be reached on Monday to Friday from 8:30 A.M. to 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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XMT